

LED1

R4 680R LED RED

R5 680R LED GREEN

R8 680R LED BLUE

3V3\_PYLK

MHPA3528RGBCT

The figure consists of two circuit diagrams. The top diagram shows the connection of the TVDD pin to a 1.2V supply and the connection of the TMS320C6701 pins to the TVDD pin. The bottom diagram shows the connection of the TMS320C6701 pins to the TVDD pin and the connection of the TVDD pin to the TVSS pin.

**Top Diagram: TVDD Pin Connection**

The TVDD pin is connected to a 1.2V supply. The TMS320C6701 pins are connected to the TVDD pin as follows:

Pin	Signal
1	T.TMS.SW.DIO
2	T.T.VCP.RX
3	T.TDI.VCP.TX
4	T.TCK.SWCLK
5	T.TRESET
6	T.TDO.SWO
7	T.TRST.VCP.RTS
8	T.TCK.SWCLK
9	T.TRESET
10	T.TDO.SWO

**Bottom Diagram: TVDD Pin Connection to TVSS**

The TVDD pin is connected to the TVSS pin. The TMS320C6701 pins are connected to the TVDD pin as follows:

Pin	Signal
1	T.TMS.SW.DIO
2	T.TDI.VCP.TX
3	T.TCK.SWCLK
4	T.TRESET
5	T.TDO.SWO
6	T.TRST.VCP.RTS
7	T.TCK.SWCLK
8	T.TRESET
9	T.TDO.SWO
10	T.TRST.VCP.RTS

[illegible]

**Pin List:**

Pin	Function	Connection
1	VBAT	3V3_PYLK
2	DIR TRST RTS	
3	DIR RESET	
4	DIR RTCK DTR	
5	PYLK_OSCIN	
6	PYLK_OSCOUT	
7	PYLK_NRST	3V3_PYLK
8	PF2-NRST	
9	VSSA	
10	VCCA	3V3_PYLK
11	5V OUT_EN	
12	T RESETa	
13	T RTCK DTRa	
14	DIR TMS SWDIOa	
15	T TMS SWDIOa OUT	
16	T TMS SWDIOa	
17	T TCK SWCLKa	
18	T TRST RTSa	
19	AD_TVDD	
20	DIR TDI VCP TX	
21	DIR TCK SWCLK	
22	DIR VCP RX	
23	VSS_1	
24	VCC_1	3V3_PYLK

**Additional Connections:**

- Pin 48:** 3V3\_PYLK
- Pin 47:** VSS\_3
- Pin 46:** 3.3V\_OUT\_EN
- Pin 45:** PYLK\_BOOT0 R27 (10K) to GND
- Pin 44:** DIR TDO SWO
- Pin 43:** PYLK\_BOOT0 R27 (10K) to GND
- Pin 42:** DIR TDO SWO
- Pin 41:** PYLK\_SPI\_MOSI
- Pin 40:** PYLK\_SPI\_MISO
- Pin 39:** PYLK\_SPI\_SCK
- Pin 38:** PYLK\_SPI\_CS
- Pin 37:** SWD\_SCK
- Pin 36:** R31 (680R) to GND
- Pin 35:** R31 (680R) to GND
- Pin 34:** SWD\_SDA
- Pin 33:** USB\_DP
- Pin 32:** USB\_DM
- Pin 31:** T VCP RXa
- Pin 30:** T TDI VCP TXa
- Pin 29:** T TDO SWOa
- Pin 28:** LED\_BLUE
- Pin 27:** LED\_RED
- Pin 26:** LED\_GREEN
- Pin 25:** TVDD\_DISCHARGE\_EN

Diagram showing TVDD Selection. A blue box labeled 'CN2' contains pins 1, 2, 3, 4, and 5. Pin 1 is connected to PYLK\_BOOT0. Pin 2 is connected to SWD\_SDA. Pin 3 is connected to 3V3\_PYLK. Pin 4 is connected to SWD\_SCK. Pin 5 is connected to a ground symbol.

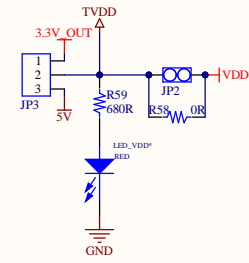
1 TVDD# P33 0P 3V3\_USB\_PYLK

The diagram shows the P25Q64SH memory chip connected to the Pico-IT8 header. The connections are as follows:

- 3V3\_PYLK** is connected to the **VDD** pin (pin 8) of the chip and to a **100nF** capacitor (C17) to ground.
- PYLK\_SPI\_CS** is connected to the **CE** pin (pin 1) of the chip through a **100k** resistor (R34).
- PYLK\_SPI\_MISO** is connected to the **MISO** pin (pin 2) of the chip.
- PYLK\_SPI\_SCK** is connected to the **SCK** pin (pin 6) of the chip.
- PYLK\_SPI\_MOSI** is connected to the **MOSI** pin (pin 5) of the chip.
- The **WP** pin (pin 4) is connected to ground.
- The **VSS** pin (pin 3) is connected to ground.
- The **HOLD** pin (pin 7) is connected to ground.

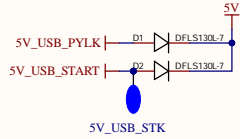


The diagram illustrates the VDD Selection circuit. It features a 3.3V\_OUT pin connected to a 5V pin via a JP3 jumper. The 3.3V\_OUT pin is also connected to a TVDD pin. A resistor R59 (680R) is connected between TVDD and a node. This node is connected to a JP2 jumper, which is also connected to a VDD pin. A resistor R58 (0R) is connected between the node and the VDD pin. A LED\_VDDP (RED) is connected between the node and GND.

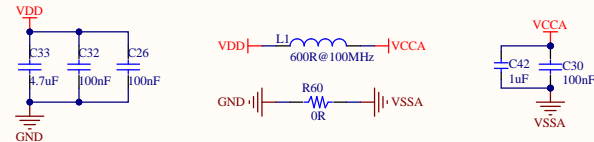
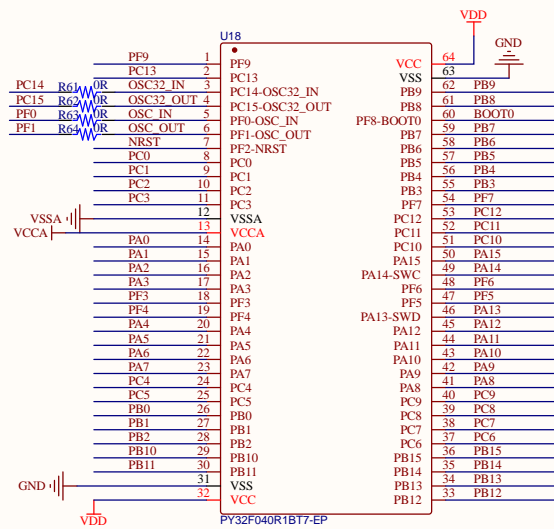


## 5V\_PWR\_Selection

The diagram illustrates a 5V\_PWR\_Selection circuit. It features two input signals, 5V\_USB\_PYLK and 5V\_USB\_START, which are connected to the inputs of a 2-to-1 multiplexer (MUX) labeled D1 and D2. The MUX is controlled by a 5V signal. The output of the MUX is connected to a 5V\_USB\_STK signal.

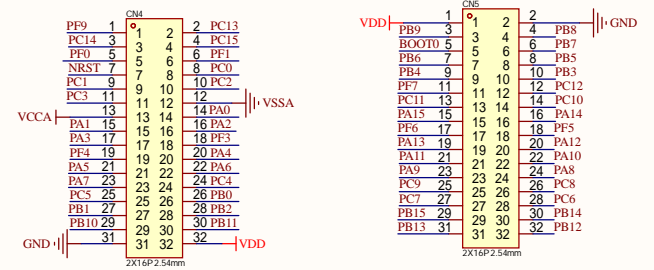
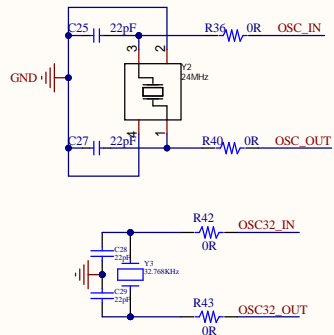


The diagram illustrates the PCB layout for the MCU interface. It features the MCU on the left, U18 (PY32F040R1BT7-EP) in the center, and various passive components like capacitors and an inductor. The MCU pins are connected to U18 pins, which are then connected to the VCC and GND planes. The layout includes a detailed pinout for U18, showing connections for VCC, VSS, and various peripheral pins. The components are labeled with their values and types, such as C33 (4.7uF), C32 (100nF), C26 (100nF), L1 (600R@100MHz), R60 (0R), C42 (1uF), and C30 (100nF).



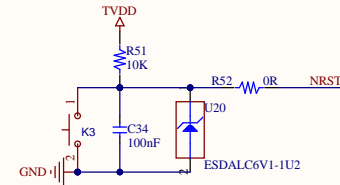
The schematic diagram shows two sections of the circuit:

- OSC Section:** This section includes a crystal oscillator circuit. It features a crystal labeled 'Y2' with a frequency of '3.68MHz'. The crystal is connected to a network of capacitors (C25, C27) and resistors (R36, R40). The input is labeled 'OSC\_IN' and the output is labeled 'OSC\_OUT'. Ground connections are indicated by a 'GND' symbol.
- OSC32 Section:** This section includes a 32kHz oscillator circuit. It features a crystal labeled 'Y3' with a frequency of '32.768kHz'. The crystal is connected to a network of capacitors (C28, C29) and resistors (R42, R43). The input is labeled 'OSC32\_IN' and the output is labeled 'OSC32\_OUT'. Ground connections are indicated by a 'GND' symbol.



### NRST

The diagram shows the NRST pin configuration. The NRST pin is connected to a 0R resistor (R52) and a 10K resistor (R51) to TVDD. It is also connected to a 100nF capacitor (C34) to GND and a diode (U20, ESDALC6V1-1U2) to GND. A switch (K3) is connected between GND and the NRST line.



## LED



BOOT\_SEL

JP4

TVDD

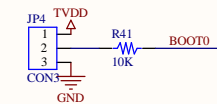
R41

10K

BOOT0

CON3

GND



## USB & POWER

